



AQ20-2424-104A
User Manual
3010002

www.aquarelasystems.com

AQ20-2424-104A 24-line 24V Output Module

User Manual

1. Specifications

- 8 bit PC104 Compatible
- 24 lines - 3 x 8-bit Ports
- Allegro UDN2987A Drivers
- 7 to 35 V
- 100 to 350 mA Output Source Current
- Internal Ground Clamp Diodes
- Over-Current Protected
- Thermal Shutdown
- LED Fault Indication
- Software Fault Detection and Reset

2. Connectors

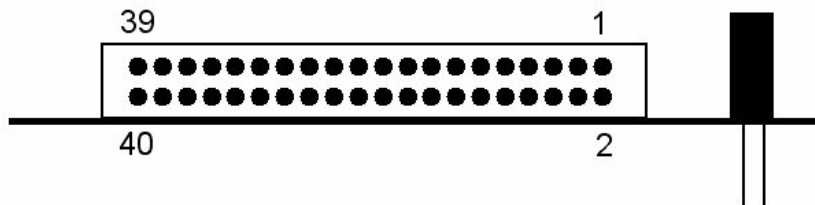


Figure 1 - JP1

Pin	Function	Pin	Function
1	Gnd	2	Power Ground
3	Gnd	4	Power Ground
5	Port C bit 8 (msb)	6	Power Ground
7	Port C bit 7	8	Power Ground
9	Port C bit 6	10	Power Ground
11	Port C bit 5	12	Power Ground
13	Port C bit 4	14	Power Ground
15	Port C bit 3	16	Power Ground
17	Port C bit 2	18	Power Ground
19	Port C bit 1 (lsb)	20	Power Ground

21	Port B bit 8 (msb)	22	Power Ground
23	Port B bit 7	24	Power Ground
25	Port B bit 6	26	Power Ground
27	Port B bit 5	28	Power Ground
29	Port B bit 4	30	Power Ground
31	Port B bit 3	32	Power Ground
33	Port B bit 2	34	Power Ground
35	Port C bit 1 (lsb)	36	Power Ground
37	+V (7 to 35V)	38	Power Ground
39	+V (7 to 35V)	40	Power Ground

Table 1 - JP1 pin functions.

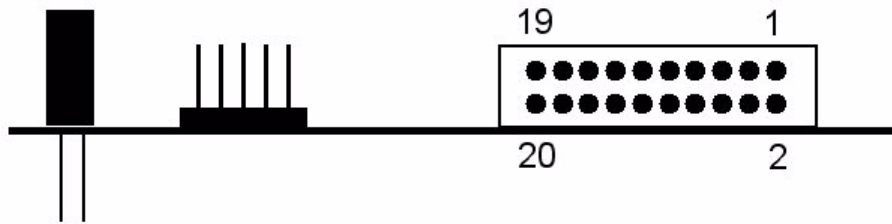
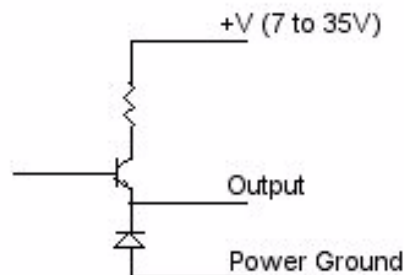


Figure 2 - JP2

Pin	Function	Pin	Function
1	Gnd	2	Power Ground
3	Port A bit 8 (msb)	4	Power Ground
5	Port A bit 7	6	Power Ground
7	Port A bit 6	8	Power Ground
9	Port A bit 5	10	Power Ground
11	Port A bit 4	12	Power Ground
13	Port A bit 3	14	Power Ground
15	Port A bit 2	16	Power Ground
17	Port A bit 1 (lsb)	18	Power Ground
19	+V (7 to 35V)	20	Power Ground

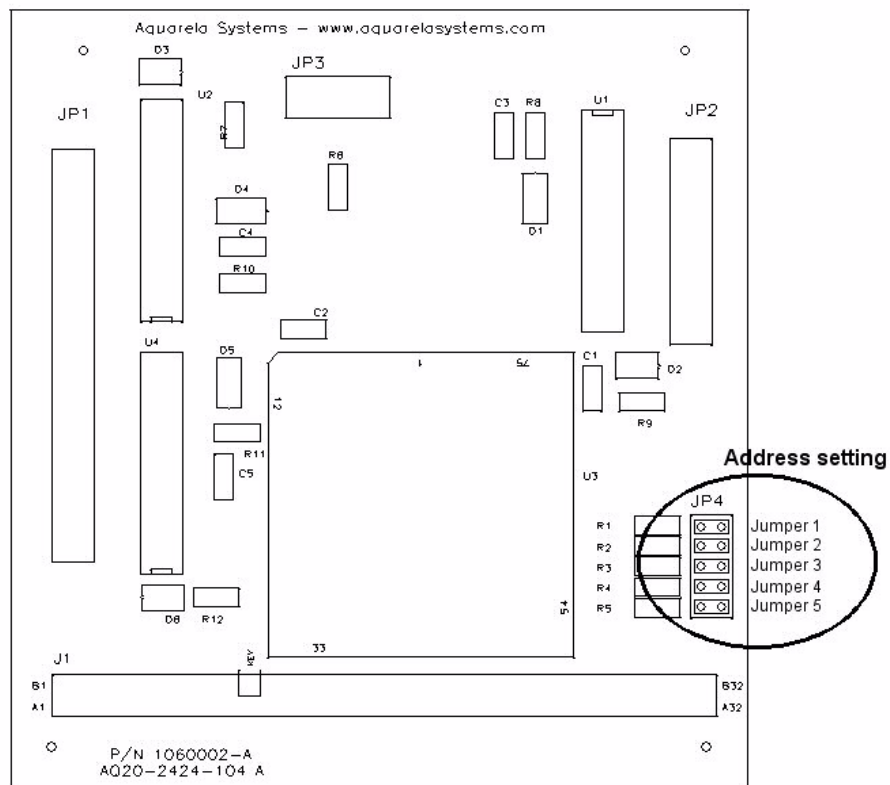
Table 2 JP2 pin functions



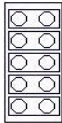
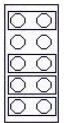
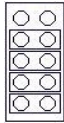
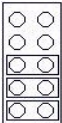
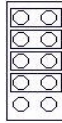
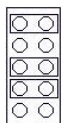
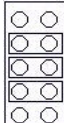
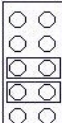
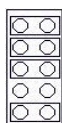
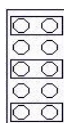
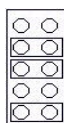
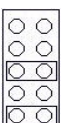
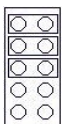
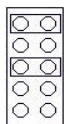
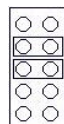
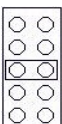
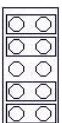

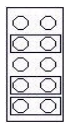
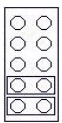

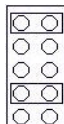
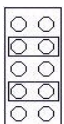
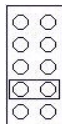
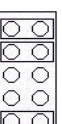

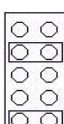
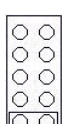

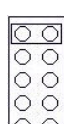
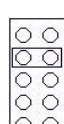

Equivalent Circuit for each Output

3. Setting the card address:

Typically a PC104 system is composed of a CPU card and one or more peripheral cards. For all the cards to operate, they must be set to different addresses. Your AQ20 24-line Output Module is provided with 5 jumpers to set the card address. These jumpers can be seen in the figure below numbered from 1 to 5.



Your card can be addressed from 0x200 (hexadecimal 200) to 0x3F0 (hexadecimal 3F0). The table below can help you set the proper address for your application

0x200 	0x280 	0x300 	0x380 
0x210 	0x290 	0x310 	0x390 
0x220 	0x2a0 	0x320 	0x3a0 
0x230 	0x2b0 	0x330 	0x3b0 
0x240 	0x2c0 	0x340 	0x3c0 
0x250 	0x2d0 	0x350 	0x3d0 
0x260 	0x2e0 	0x360 	0x3e0 
0x270 	0x2f0 	0x370 	0x3f0 

4. Functions:

After setting the base address of your AQ20-2424-104A card, four address positions will be used at BASE+0, BASE+1, BASE+2 and BASE+3.

BASE+0 is a read/write register. All the others are write only.

BASE+0 write:

Res	Res	Res	Res	Res	RSTPC	RSTPB	RSTPA
-----	-----	-----	-----	-----	-------	-------	-------

Res - Reserved

RSTPA - Port A Enable / Fault Reset - Set to 1 to enable Port A

RSTPB - Port B Enable / Fault Reset - Set to 1 to enable Port B

RSTPC - Port C Enable / Fault Reset - Set to 1 to enable Port C

BASE+0 read:

Res	Res	Res	Res	Res	FPC	FPB	FPA
-----	-----	-----	-----	-----	-----	-----	-----

Res - Reserved

FPA - Port A Status (Fault = 1 OK = 0)

FPB - Port B Status (Fault = 1 OK = 0)

FPC - Port C Status (Fault = 1 OK = 0)

BASE+1 write - PORT A (JP2)

bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
JP2-3	JP2-5	JP2-7	JP2-9	JP2-11	JP2-13	JP2-15	JP2-17

BASE+2 write - PORT B (JP1)

bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
JP1-21	JP1-23	JP1-25	JP1-27	JP1-29	JP1-31	JP1-33	JP1-35

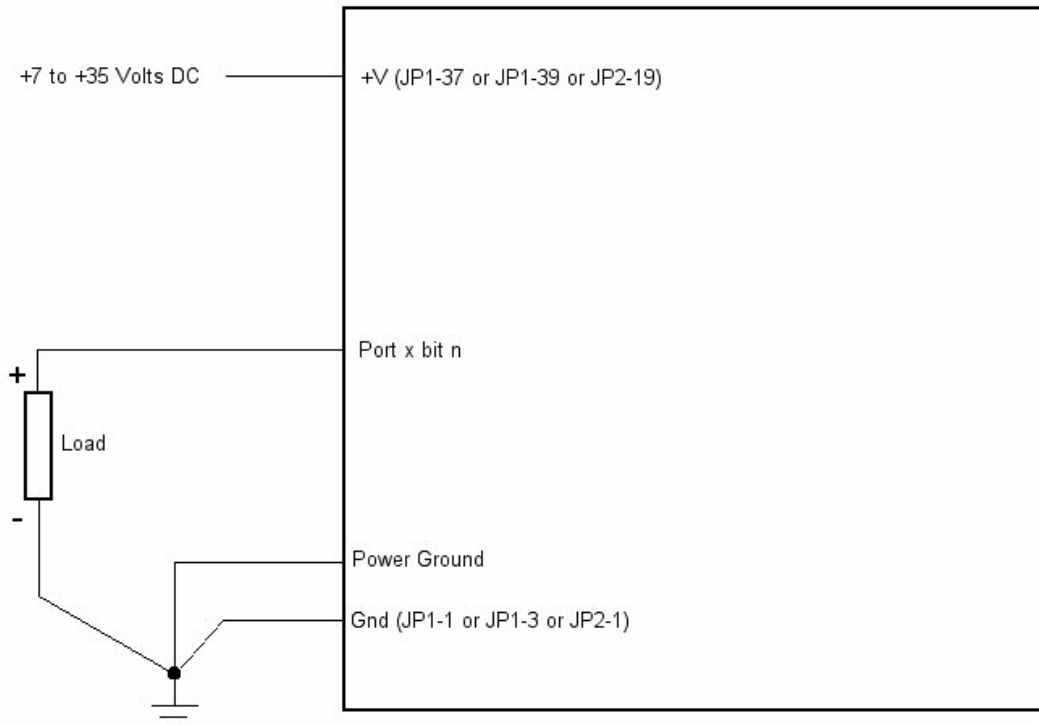
BASE+3 write - PORT C (JP1)


bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
JP1-5	JP1-7	JP1-9	JP1-11	JP1-13	JP1-15	JP1-17	JP1-19

5. Connections:

You can connect up to 24 loads to your card. The load power supply (7 to 35V) must be connected to JP1-37, JP1-39, and JP2-19. All these pins are internally connected. There is one individual Power Ground for each output, but they are interconnected.

The power (+5V) and ground for the logic section is supplied by the PC104 connector (J1) but for the system to operate the logic ground (Gnd JP1-1, JP1-3 and JP2-1) must be connected to Power Ground. To improve noise immunity, they should be connected to a single point low resistance ground.



	AQ20-2424-104A User Manual 3010002	www.aquarelasystems.com
---	--	--

6. Protections:

6.1 Short Circuit

Each bit is individually protected against short-circuit and overload. The trip point is specified at 370mA. Only the offending bit is shut down. The remaining of the port will continue to work. The Port red fault LED will turn on and the corresponding Port Status bit (PFx) will read as 1.

To reset the fault you should write 0 to the corresponding Port Enable/Reset bit (RSTPx) and then write 1 to enable it again.

6.2 Thermal Overload

Ports are protected against thermal overload. If the driver temperature exceeds 165 C the Port will shutdown. The Port red fault LED will turn on and the corresponding Port Status bit (PFx) will read as 1.

To reset the fault you should write 0 to the corresponding Port Enable/Reset bit (RSTPx) and then write 1 to enable it again.